

# FUNCTIONAL PATTERN LOGIC DIAGNOSTIC METHOD

## Abstract of the Disclosure

A method of diagnosing complex semiconductor device functional testing failures by combining deterministic and functional testing with diagnostic techniques. The method determines the failing logic locations by creating a new test pattern based on the functional failure by transforming a functional pattern into a scan deterministic pattern so that existing diagnostic tools can also be used to determine the location of and type of error in the failing circuit without impacting manufacturing test. This is accomplished by identifying the failing vector during the functional test, observing the states of the failed device by unloading the values of the latches from the LSSD scan chain before the failing vector. This may include reading the embedded circuit memories and other circuit storage elements, generating a LOAD from the unloaded states of the latches, applying the generated LOAD as the first event of a newly created independent LSSD deterministic pattern, applying the same identical primary inputs and Clocks that produced the failure to a correctly operating device using the bootstrapping technique, unloading the output of the correctly operating device to generate a deterministic LSSD pattern; and applying the generated deterministic LSSD pattern to the failing device to diagnose the failure using existing LSSD deterministic tools.